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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/998,830	12/03/2001	Taiyuu Miyamoto	027260-504	7164

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EXAMINER	
RIZZUTO, KEVIN P	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 11/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/998,830	MIYAMOTO, TAIYUU	
	Examiner	Art Unit	
	Kevin P Rizzuto	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5,6 and 8* is/are pending in the application.

4a) Of the above claim(s) *3,4 and 7* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,6 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-2, 5-6 and 8 have been examined.

2. Acknowledgement of papers filed: Amendment on 9/2/2005. The papers filed have been placed on record.

Specification

3. The amended title of the invention remains non-descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 5-6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sibigtroth et al., U.S. Patent 5,251,304, herein referred to as Sibigtroth.

6. As per claim 1, Sibigtroth teaches a microcomputer comprising:

-A memory (Programmable Security Device 20 and Memory 13), a central processing unit (Data Processor 14):

-And a functional block comprising: a peripheral block (External Peripheral 12, Instruction Inhibit 18) built-in said microcomputer, wherein said memory has a

reprogrammable nonvolatile memory: (Column 3, line 61 to column 4, line 6), in which a lock code is written in a specified area (Enable signal);

-And the microcomputer comprises:

-A first decoding circuit connected with said nonvolatile memory, which reads out said lock code, and decodes said lock code: (The Inverter 50 (figure 2) reads out the enable signal and decodes it.)

-A logic circuit that performs a predetermined operation on an externally input mode bit (Instruction Fetch signal, figure 2), by the output from the first decoding circuit: (The logic circuit (And gate 52) takes in the decoded enable bit and Instruction Fetch bit, which is external to all circuits shown in Figure 1, including external to the Instruction Inhibit 18 unit).

-And a second decoding circuit that decodes the processed mode bit by receiving the output from said logic circuit, and sends the obtained results to said functional block. (The OR circuit 54 is the second decoding circuit, which decodes the bit output from the logic circuit (AND 52), and sends its output to the functional block (the logic within Instruction Inhibit 18 other than items 50, 52 and 54)).

See also Column 3, lines 61 to column 4, lines 32

7. Sibigtroth fails to teach wherein the reprogrammable nonvolatile memory holds user data along with the lock code.

8. However, Examiner takes Official Notice that reconfigurable nonvolatile memories are well known in the art to store multiple types and instances of important data that needs to be saved even after power is removed from the system.

9. It would have been obvious to one of ordinary skill in the art at the time the invention was made to store additional user data in the reprogrammable nonvolatile memory (Programmable Security Device 20) since Examiner takes Official Notice memories are well known in the art to store multiple types and instances of important data that needs to be saved even after power is removed from the system.

10. As per claim 2, Sibigtroth teaches the microcomputer of claim 1, wherein said logic circuit consists of an AND circuit (Figure 2, AND gate 52).

11. As per claim 5, Sibigtroth teaches a microcomputer comprising:

-A memory (Programmable Security Device 20), a central processing unit (Data Processor 14),

-A functional block comprising: a peripheral block, built-in said microcomputer, and an external terminal: (The External Peripheral 12 and Instruction Inhibit 18, the Instruction Inhibit 18 receives external signals (bus 30, enable and Instruction Fetch) on external terminals.)

-Wherein said memory comprises a reprogrammable nonvolatile memory, in which a function-selecting code for selecting the function of the external terminal is written in a specified area: (Column 3, line 61 to column 4, line 6), the Enable signal is stored within the Programmable Security Device 20 and is used for selecting a function

of the external terminal connecting the Instruction Inhibit 18 and the External Peripheral 12 (Data/Instruction Bus 30).)

-And said microcomputer comprises: a first decoding circuit connected with the nonvolatile memory, which reads out said function-selecting code and decodes this code: (The Inverter 50 (figure 2) reads out the enable signal and decodes it.)

-And a selector circuit that selects a function of the external terminal by receiving the output from said first decoding circuit: (The selector circuit (And gate 52) takes in the decoded enable bit and Instruction Fetch bit, and based on the output of the AND gate 52, the external terminal (shown in figure 2) performs different functions, i.e., either allowing the bus 30 to connect to the Data bus 24 or not allowing. Column 3, lines 61 to column 4, lines 32).

12. Sibigtroth fails to teach wherein the reprogrammable nonvolatile memory holds user data along with the function selecting code.

13. However, Examiner takes Official Notice that reconfigurable nonvolatile memories are well known in the art to store multiple types and instances of important data that needs to be saved even after power is removed from the system.

14. It would have been obvious to one of ordinary skill in the art at the time the invention was made to store additional user data in the reprogrammable nonvolatile memory (Programmable Security Device 20) since Examiner takes Official Notice memories are well known in the art to store multiple types and instances of important data that needs to be saved even after power is removed from the system.

15. As per claim 6, Sibigtroth teaches a microcomputer comprising a memory, a central processing unit:

-And a functional block comprising a peripheral block (External Peripheral 12, Instruction Inhibit 18), built-in said microcomputer, wherein said memory (Programmable Security Device 20) comprises a reprogrammable nonvolatile memory (Column 3, line 61 to column 4, line 6), in which a limiting code for limiting a command is written in a specified area: (Enable signal)

-And said microcomputer comprises: a first decoding circuit connected with said nonvolatile memory, which reads out said limiting code, and decodes this code: (The Inverter 50 (figure 2) reads out the enable signal and decodes it.)

-And a second decoding circuit that limits a command to be used, by the output from said first decoding circuit. (The second decoding circuit (And gate 52) takes in the decoded Enable bit and Instruction Fetch bit, and based on the output of the AND gate 52, the external terminal (shown in figure 2) performs different functions, i.e., either allowing the bus 30 to connect to the Data bus 24 or not allowing (and therefore limiting commands to be used). (Column 3, lines 61 to column 4, lines 32)

16. Sibigtroth fails to teach wherein the reprogrammable nonvolatile memory holds user data along with the limiting code.

17. However, Examiner takes Official Notice that reconfigurable nonvolatile memories are well known in the art to store multiple types and instances of important data that needs to be saved even after power is removed from the system.

18. It would have been obvious to one of ordinary skill in the art at the time the invention was made to store additional user data in the reprogrammable nonvolatile memory (Programmable Security Device 20) since Examiner takes Official Notice memories are well known in the art to store multiple types and instances of important data that needs to be saved even after power is removed from the system.

19. As per claim 8, Sibigtroth teaches the microcomputer of claim 1, wherein said reprogrammable nonvolatile memory consists of a data memory and a program memory. (Memory 13, a portion of the memory from claim 1, contains both instructions a data and is reprogrammable (column 3, lines 3-8). However, It is not stated that Memory 13 is also non-volatile.

20. However, Examiner takes Official Notice that designing memories as non-volatile allows data and instructions to remain on the disk when the power is removed, and it is well known in the art to design memories as non-volatile for this purpose.

21. It would have been obvious to one of ordinary skill in the art at the time the invention was made to design the memory 13 as non-volatile since Examiner takes Official Notice that it is well known to design memories as non-volatile memories so that they can retain data when their power is removed. This would cause the entire memory (memory 13 and Programmable Security Device 20) to be reprogrammable and nonvolatile, and to contain both data and instructions.

22. As per claim 8, Sibigtroth teaches the microcomputer of claim 1, wherein said reprogrammable nonvolatile memory consists of a data memory and a program memory. (From another point of view than the above rejection of claim 8, While

Programmable Security Device is both reprogrammable and nonvolatile (column 3, line 61 to column 4, line 32), it alone does not contain both data and instructions.)

23. However, Sibigtroth suggests the any memory device may be used for Programmable Security Device 20.

24. It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the Programmable Security Device 20 with the Memory 13 since it has been held use of one piece construction instead of the reference structure is matter of obvious engineering choice (In re Larson, 340 F.2d 965, 967, 144 USPQ 347, 349 (CCPA 1965); and In re Wolfe, 251 F.2d 854, 855, 116, USPQ 443, 444 (CCPA 1958)) and since Sibigtroth suggests that any memory device can be used to as the Programmable Security Device 20.

25. Integrating the memories would cause there to be one reconfigurable, non-volatile memory which contains both the lock code (data) and other data and instructions.

Response to Arguments

26. Applicants arguments filed on 9/2/2005 have been fully considered but they are not persuasive.

27. Applicant argues the novelty/rejection of claims 1 and 5-7

a. "Thus, Sibigtroth et al merely discloses a security device 20 which stores the state of an Enable signal. (col. 4, lines 1-) Nothing in Sibigtroth et al shows, teaches or suggests a nonvolatile memory storing user data and one of a lock

code, function-selecting code or limiting code as claimed in claims 1, 5 and 6. Rather, Sibigtroth et al merely discloses a security device 20 storing the state of an Enable signal."

28. These arguments are not found persuasive for the following reasons:

b. To clarify, applicant's attention is directed towards the new 35 U.S.C. 103 Rejection above. As is shown above, merely storing "user data" on the nonvolatile memory of Sibigtroth in addition to the enable code is an obvious variation and thus does not patentably distinguish the claim over the prior art. Storing user data on non-volatile memory was well known in the art and is very commonly used since data can be stored in the memory even after power is removed from the processor system.

29. Applicant argues the novelty/rejection of claims 1 and 5-7

c. "Additionally, Sibigtroth et al merely discloses an AND gate 52 receiving a Fetch signal from decoder 16 which is part of an integrated circuit package portion 11 which includes the decoder 16 and instruction inhibit circuit 18. (col. 2, lines 18-25, col. 3, lines 46-49) In other words, the Fetch signal from decoder 16 is not an external input mode bit. Therefore, nothing in Sibigtroth et al shows teaches or suggests a logic circuit that performs a predetermined operation on an external input mode bit as claimed in claim 1. Rather, Sibigtroth et al teaches away from the claimed invention since the decoder 16 and instruction inhibit circuit 18 are provided in the same single integrated circuit package portion, and the instruction Fetch signal output by the decoder 16 is an internal signal."

30. These arguments are not found persuasive for the following reasons:

d. To clarify, applicant's attention is directed towards the 35 U.S.C. 103 rejection above where each limitation regarding the external signal is met by Sibigtroth. The pertinent portions of the rejection are copied below for convenience.

i. -A logic circuit that performs a predetermined operation on an externally input mode bit (Instruction Fetch signal, figure 2), by the output from the first decoding circuit: (The logic circuit (And gate 52) takes in the decoded enable bit and Instruction Fetch bit, which is external to all circuits shown in Figure 1, including external to the Instruction Inhibit 18 unit).

e. To further clarify, in figure 1 the Instruction Fetch signal is output from the Decoder 16 and *input* to the Instruction Inhibit 18. Since it is *input* to the Instruction Inhibit circuit 18 (shown in detail in figure 2), it is inherent that it was *external* to the Instruction Inhibit circuit 18 and the logic circuit (AND gate 52). Therefore, it is shown that the Instruction Fetch signal is in fact an "externally input mode bit" as claimed.

Conclusion

31. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin P Rizzuto whose telephone number is (571) 272-4174. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

KPR

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